

Hypothetical Modelling of SRAM Using Spin Degree of Freedom

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ABSTRACT: *Consequence of electron mobility is a pivotal study in low power consuming device research. Single Spin Logic (SSL) is an optimal solution derived from Spintronics that also usher a new horizon in device research, without tangling over the only charge of an electron. It resonates the notion of spin degree of freedom and the vicinity of electron coherence. Thus SSL popularized from simple logic gates to modern complex circuits. One such endeavor is reported here by the authors categorized spin for SRAM designing. The modus operandi is deliberated within the limits of spin polarization. The effectual linkage of electron transport phenomena is proficiently carried out in the orbit of spin where each unit of SRAM is SSL oriented*

Keywords: *SSL, Spintronics, Decoder, D flip flop, Static Random Access Memory (SRAM).*

I. INTRODUCTION

In Present day, Scaling down of electron components is a great challenge to the researchers. In this regard in 1965 Gordon Moore deliberated that the number of transistor per square inch doubles in every year. But it also suffers from different problems like physical economical and technological challenges. Eventually a new concept was revolutionized namely nanoelectronics [1] in which one can control the movement and position of a small number of electrons. Carbon Nano Tubes (CNT), Rapid Single Flux Quantum (RSFQ), Resonant Tunneling Devices (RTD), Quantum Dots (QD), Single Electron Transistor (SET) are some examples of these nanodevices among which SET is popularized owing to nano scale feature size, its ultra-low power dissipation and Coulomb Blocked Oscillation like features.

But SET alike other charge based devices suffers from leakage power. To overcome this problem another novel technology deliberated by Prof. Supriyo Bandyopadhyay was incorporated namely 'Spintronics' i.e., spin based electronic [2]. In spintronics, logic can be changed by spin orientation or by changing the spin of electron. At the same time, Sarkar et al. documented the spin properties in logic designing and the term SSL [3] was coined. Consecutively, several logical operations like NAND [4], Full Adder [5], Multiplexer [6], Reversible Logic Gates [7], ALU [8] etc was implemented by SSL.

On the other hand, memory elements are very essential for data storage. In memory designing Giant Magneto Resistance (GMR) [9] is designed to hold bulk information. But it shows some difficulties for designing small size memory. To overcome this problem the authors emphasized to implement the memory that can store semi bulk information and for this the authors adhered in using SSL purposely in SRAM. Rather a new type of memory device is hypothecated i.e, SSL-SRAM.

II. OVERVIEW OF SRAM

SRAM [10] stored data as long as the power supply is on. It stores the data in logical form i.e. either '0' or '1'. Here SRAM is designed by using decoder and flip flops. Decoder selects the single word at a time and flip flop is used to store the data synchronously. Let us consider that a 4-bit data has to be transferred from transmitter to receiver. Thus a 16 messages (0000 to 1111) are to be transmitted. To make it more compact the authors intently truncated this sub section. The insight was given in SSL-SRAM modelling.

III. SPIN REALIZATION OF DECODER AND D FLIP FLOP

Decoders [11] are used as data selectors. Table 1 shows the truth table of a 2:4 decoder and Fig. 1 shows the same. Here A and B are two inputs and D₀, D₁, D₂, D₃ are the four outputs being generated. In all SSL realization figures blue arrows shows the inputs and green arrows represents the outputs. The decoder at a time process a single output depending upon the inputs. Fig 2 shows the scholastic spin realization of decoder outputs when A=1 (represented by up spin '↑') and B=0 (represented by down spin '↓')

Table 1: Truth table of Decoder

Inputs		Outputs			
A	B	D ₃	D ₂	D ₁	D ₀
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

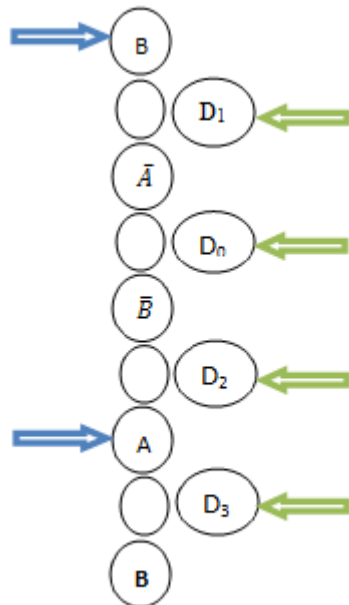


Fig. 1: SSL realization of decoder

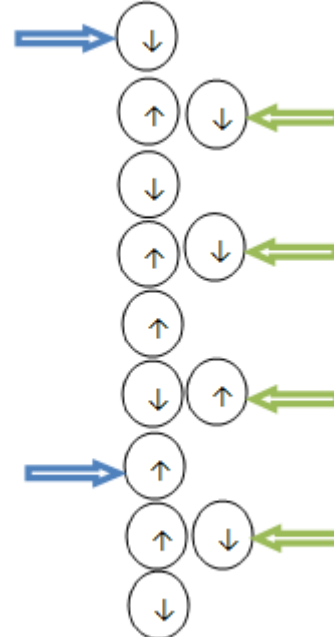


Fig. 2 : SSL based decoder for special case

On the other hand flip flop enacts as a single bit storage device. Furthermore, D flip flops [12] are indispensable because it has equal number of inputs and outputs. So D flip flop can be easily used in SRAM for data storage. The truth table for D flip flop is given in Table 2 and the spin realization of the same is given in Fig.3

Table 2: Truth table of D Flip

Present state	Input (D)	Next state	
		Q	\bar{Q}
0	0	0	1
0	1	1	0
1	0	0	1
1	1	1	0

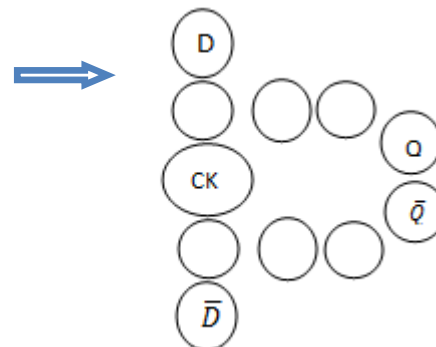


Fig. 3: SSL realization of D Flip flop

IV. SSL BASED SRAM

Fig. 4 gives the overall idea of a SRAM where a 4:16 decoder and few D flip flops are involved. This 4:16 decoder is designed by using five 2:4 decoders. Two higher order inputs say A and B, of the decoder are used as ‘primary selection’ and four output of it are used as ‘Enable Line’ of other four secondary decoders. As we know that in decoder circuit a single output is enabled so instantaneously four outputs of primary decoder can be activated using a single secondary decoder at that instant. The other two inputs say C and D are used for final selections. Then D flip flops are used to process the output of each decoder to store the final data of SRAM.

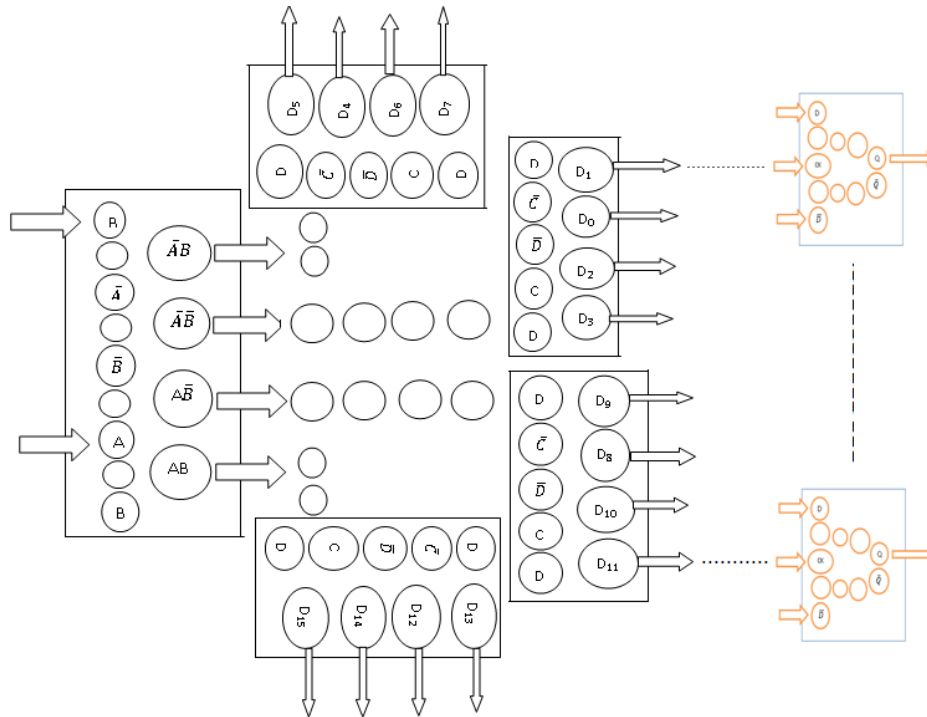


Fig. 4: SSL realization of SRAM

V. CONCLUSION

From the above discussion we can say that SSL based design offers light weight, high operating speed, and low cost, long duration battery operation like advantages and thus makes it more acceptable in SRAM design. More conveniently the affects of GMR is limited. Henceforth modeling of SRAM using SSL is ubiquitous in the realm of next generation memory designing. Apparently the mobility of data transfer is nearly equal to the electronic speed in this SSL SRAM. Conversely the propagation delay is minimalized manifold in the proposed architecture.

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